## IN THE CLAIMS

Please amend the claims as stated below:

1-22. (Cancelled)

23. (Currently Amended) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a high speed interconnect;

a management interconnect;

a first cell and a second cell, each cell comprising at least one processor coupled to

at least one random-access memory subsystem,

at least one nonvolatile memory system, and

a high-speed interconnect interface coupled to the high speed interconnect;

the first cell and second cell further comprise:

a management processor coupled to a nonvolatile memory for management code, and

an interface to the management interconnect

wherein the nonvolatile memory subsystem of the first cell has recorded therein errored firmware selected from the group consisting of outdated or corrupt firmware, and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware; and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is errored firmware and, upon recognizing that the firmware of the first cell is errored, for transmitting over the management interconnect a request for valid firmware to the second cell, and for updating the nonvolatile memory system of the first cell with valid firmware;

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is

valid, and for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell; and

wherein the management code of the second cell comprises machine readable code to receive a request for valid firmware and, in response thereto, to transmit an acknowledgement via the ~~manageability system~~ management interconnect, to enable the high speed interconnect; and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

24. (Previously Presented) The cellular computer system of claim 23 wherein the errored firmware is corrupt firmware.

25 (Previously Presented) The cellular computer system of claim 23 wherein the errored firmware is outdated firmware.

26. (Currently Amended) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a high speed interconnect;

a management interconnect;

a first cell and a second cell, each cell comprising at least one processor coupled to at least one random-access memory subsystem,

at least one nonvolatile memory system, and

a high-speed interconnect interface coupled to the high speed interconnect;

the first cell and second cell further comprise:

a management processor coupled to a nonvolatile memory for management code, and

an interface to the management interconnect

wherein the nonvolatile memory subsystem of the first cell has recorded therein errored firmware selected from the group consisting of outdated or corrupt firmware, and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware; and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is errored firmware and, upon recognizing that the firmware of the first cell is errored, for transmitting over the management interconnect a request for valid firmware to the second cell, and for updating the nonvolatile memory system of the first cell with valid firmware;

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid, and for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell; and

wherein the management code of the second cell comprises machine readable code to receive a request for valid firmware and, in response thereto, to transmit an acknowledgement via the ~~manageability system~~ management interconnect, to enable the high speed interconnect; and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the manageability system interconnect.

27. (Previously Presented) The cellular computer system of claim 26 wherein the errored firmware is corrupt firmware.

28 (Previously Presented) The cellular computer system of claim 26 wherein the errored firmware is outdated firmware.

29. (New) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a high speed interconnect;

a management interconnect;

a first cell and a second cell, each cell comprising at hardware level:

at least one processor of the cell coupled to at least one random-access memory subsystem of the cell,

at least one nonvolatile memory system coupled to the at least one processor of the cell,

a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect,

a management processor of the cell coupled to a nonvolatile memory for management code of the cell, and

an interface coupling the management processor of the cell to the management interconnect;

wherein the nonvolatile memory subsystem of the first cell has recorded therein errored firmware selected from the group consisting of outdated or corrupt firmware, and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware; and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is errored firmware and, upon recognizing that the firmware of the first cell is errored, for transmitting over the management interconnect a request for valid firmware to the second cell, and for updating the nonvolatile memory system of the first cell with valid firmware;

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid, and for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell; and

wherein the management code of the second cell comprises machine readable code to receive a request for valid firmware and, in response thereto, to transmit an acknowledgement via the management interconnect, to enable the high speed interconnect; and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

30. (New) The cellular computer system of claim 29 wherein the errored firmware is corrupt firmware.

31 (New) The cellular computer system of claim 29 wherein the errored firmware is outdated firmware.